Electrical Characterization of MOSFETs from a 180 nm CMOS Technology

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Abstract **- This work objective the electrical characterization of MOSFETs from a 180nm CMOS Technology offered by Taiwanese company United Microelectronics Corp. (UMC). The study is based on electrical measurements of the drain current versus gate voltage and the drain current versus drain voltage. Devices with variable channel length and channel width have been measured.**

Keywords - MOSFET, CMOS, drain current, threshold voltage.

I. INTRODUCTION

MOSFETs are electronic devices that follow the Metal-Oxide-Semiconductor (MOS) technology with field effect. More usually MOS is constructed of monocrystalline silicon wafers, which serve as physical support for the device, and are manufactured on a p-type substrate (i.e., mostly with positive moving charges). Pure silicon has a structure formed by four valence electrons associated with each of the silicon atoms. To modulate the conductivity of silicon, it is necessary to insert impurities, which will react with silicon electrons. These impurities will break a covalent bond and, depending on their number of electrons, will give rise to n-type materials, if pentavalent impurities are used, or p-type if trivalent impurities are used [1].

Circuits in CMOS technology are build using pMOS and nMOS transistors. Figure 1 shows the schematic cross-section representation of a CMOS pair, consisting of n-type (nMOS) and p-type (pMOS) MOS transistors. In this figure are also indicated the electrodes of the drain (D), gate (G), source (S), and bulk (B) of each transistor.

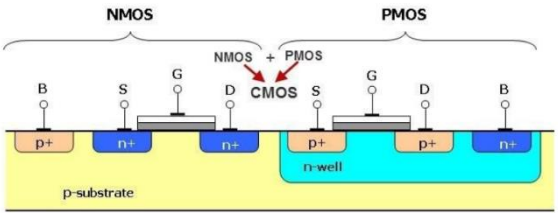

Figure 1 - Transverse profile of transistors nMOS and pMOS, indicating the electrodes of the drain, gate, source, and bulk.

In the case of nMOS transistors, for gate voltages higher than the threshold voltage (or smaller in case of pMOS), the devices operate in the triode region or the saturation region, depending on the voltages applied to their terminals.

Figure 2 represents the Triode region and the Saturation region.

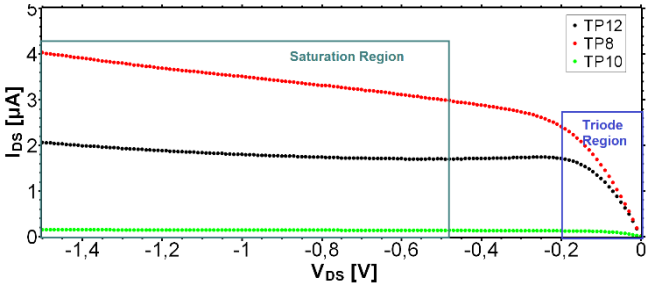

Figure 2 - Triode and Saturation region.

The device operates in the triode region when $V_{DS}<V_{GS}-V_T$. In this operational region, there exists an inversion layer that extends from source to drain electrodes. The drain current (I_{DS}) of nMOS transistor operating in the triode region can be described by equation (1) [1]:

$$I_{DS} = \mu_n C_{ox} \left(\frac{W}{L}\right)\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \quad (1)$$

where µn is the mobility of electrons, V_{GS} is the gate voltage, V_{DS} is the drain voltage and C_{OX} is the gate oxide capacitance per unit of area.

The device operates in saturation region when $V_{DS}>V_{GS}-V_T$. In this region the inversion layer is smaller than the channel length, which reduces the device output conductance with the drain bias.

The drain current (I_{DS}) of nMOS transistor operating in the saturation region can be described by equation (2) [1]:

$$I_{DS} = \mu_n C_{ox} \left(\frac{W}{L}\right)\frac{(V_{GS} - V_T)^2}{2}(1+\lambda V_{DS}) \quad (2)$$

where λ is the channel length modulation factor.

Within the electrical parameters that are possible to extract from the component, one of the most important [2] is the threshold voltage (voltage at which the transistor begins to conduct – V_T), which is proportional to the doping concentration and dependent on the device dimensions of channel length (L) and channel width (W). When the channel length is reduced, due to the proximity of the source and drain terminals, the source and drain

depletion regions extend under the channel so that the depletion charge below the gate is no longer controlled only by the gate potential, i.e., the shorter the channel length, the smaller the V_T. This is usually referred to as short-channel effect (SCE). One technological solution to SCE is the ion implantation of majority carriers obliquely to the gate, giving rise to the region called "Pocket", where there is a higher doping concentration [3]. Because of this higher doping concentration, the so-called phenomenon of reverse short channel effect (RSCE) emerged, i.e., the shorter the channel length, the higher the threshold voltage, due to the increase in the average concentration of dopants with shorter channel length [5].

I.1 Device Structure and Methodology

Drain current as a function of gate voltage and drain current as a function of drain voltage measurements were performed in individual nMOS and pMOS transistors fabricated in using the CMOS technology of 180 nm of minimum channel length from UMC foundry [4] with gate oxide thickness of 4nm.

For a better understanding, transistors were divided into four groups:

a) TN1 and TP1, with the shortest channel length (L=0,18 µm) and channel width;
b) TN2 to TN7 and TP2 to TP7, with constant W and L variable. (W= 3,00µm);
c) TN8 to TN11 and TP8 to TP11, with constant L and W variable. (L=1,00µm);
d) TN12 and TP12, with the longest length and channel width (L=W=10,00µm).

Table I presents the dimensions of the transistors and a photograph of the test-chip is presented in Figure 3, identifying the various structures available. Table I also presents the results of the threshold voltage of each mentioned nMOS and pMOS transistors. The V_T has been obtained through the second derivative method.

Table I – Summary of the transistor´s dimensions available in the test-chip and their threshold voltages.

Device	L (µm)	W (µm)	Threshold voltage [V]
TN1, TP1	0.18	0.24	0.54, -0.53
TN2, TP2	0.18	3.00	0.52, -0.53
TN3, TP3	0.24	3.00	0.51, -0.51
TN4, TP4	0.30	3.00	0.52, -0.53
TN5, TP5	0.40	3.00	0.52, -0.52
TN6, TP6	0.60	3.00	0.51, -0.54
TN7, TP7	1.00	3.00	0.55, -0.49
TN8, TP8	1.00	1.00	0.57, -0.54
TN9, TP9	1.00	0.50	0.54, -0.54
TN10, TP10	1.00	0.30	0.51, -0.53
TN11, TP11	1.00	0.24	0.51, -0.56
TN12, TP12	10.00	10.00	0.54, -0.54

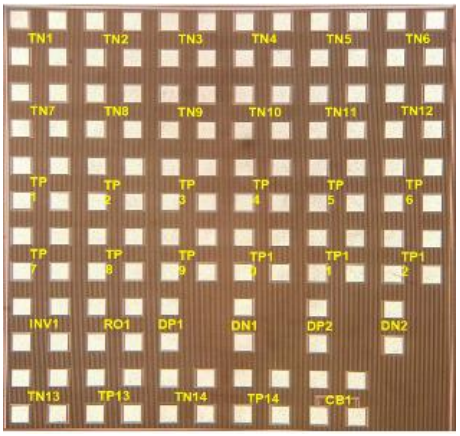

Figure 3 - Photograph of Test-Chip identifying the devices indicated in Table I

II. RESULTS AND DISCUSSION

Figure 4 shows as curves of the $I_{DS}/(W/L)$ as a function of V_{GS}-V_T, obtained with a drain voltage $|V_{DS}|$= 50mV, for transistors TN1 and TN12, TP1 and TP12.

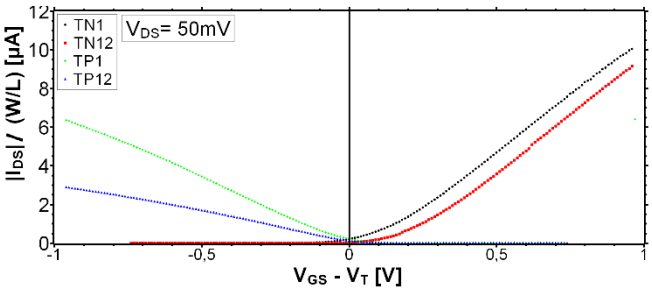

Figure 4 - $|I_{DS}|/(W/L)$ x V_{GS}- V_T curves, measured with $|V_{DS}|$=50 mV for transistors TN1 and TN12, TP1 and TP12.

The $|I_{DS}|$ of both nMOS transistors is higher than that of the pMOS transistor with similar dimensions and bias conditions. This effect is associated with carrier mobility, as μ_n is higher than μ_p (hole mobility).

As indicated by equation (1), for the same V_{GS}-V_T the $|I_{DS}|/(W/L)$ curves should be superposed. However, two distinct effects appear in Fig. 4 to be noticed: for the same transistor type, the normalized current is larger in the shorter transistor than in longer ones. This difference is caused by the doping concentration and their resulting carrier mobility.

The curves of Figure 4 were plotted using the effective values of $\frac{W}{L}$ obtained after the fabrication of the devices instead of their nominal values of 1.333 for transistors TN1 and TP1, and of 1.0 for transistors TN12 and TP12. The effective value of $\frac{W}{L}$ is important especially from smaller length channel transistors. The average of the tree chips was used to obtain the results of 1.68 to pMOS and 1.182 to nMOS.

Figure 5 shows the curves of the $|I_{DS}|$* L as a function of V_{GS}, obtained with a drain voltage of $|V_{DS}|$ = 50mV, for transistors with variable L and W = 3µm.

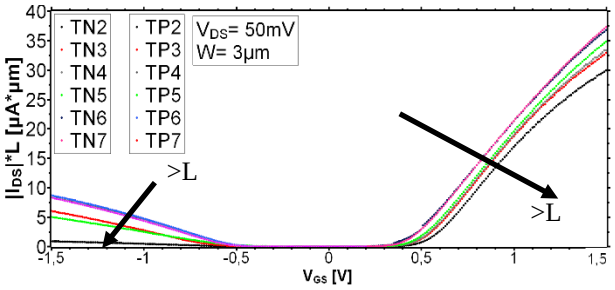

Figure 5- Curves $|I_{DS}|$*L x V_{GS} for transistors with constant channel width and variable L.

The curves of figure 5, which represent group b), shows that the reduction of L causes a decrease in the $|I_{DS}|$*L current. By multiplying the drain currents by L, as shown in Fig. 5, it appears that the highest current represents the TN7 or TP7 transistors, which have the longest channel length in the group.

Even though the devices had the same bias voltage and they were in the sataration region (2), the drain current drecreases compared with the TP7 and TN7 transistors. This current reduction is associated with an increase in the doping concentration for devices with shorter L, associated with the formation of the pocket region. With a higher concentration of impurities, there is smaller carrier mobility and higher threshold voltage.

Figure 6 shows the curves of the $|I_{DS}|/W$ as a function of V_{GS}, obtained with drain voltage $|V_{DS}|$ = 50mV, for all transistors with variable W and L = 1 µm.

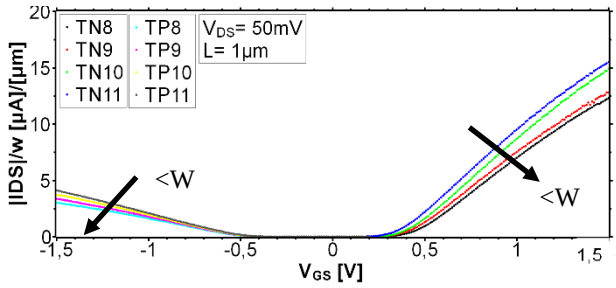

Figure 6 - Curves $|I_{DS}|/W$ x V_{GS} transistors with constant channel length.

This curve represents group c) and shows an increase in $|I_{DS}|/W$ with an increase in channel width. Similarly, to what was seen in figure 5 for shorter L, due to the increase in the concentration of impurities for smaller widths, the drain current is higher with higher W because of their higher mobility.

The measurements of the drain current as a function of the drain voltage were performed with constant gate voltage. However, to facilitate the comparison between devices with different V_T, the gate voltage overdrive (V_{GT}= V_{GS} - V_T) has been kept constant. The value of V_{GT} used was 0.2V.

The curves obtained in figure 7 and 8 shows how the drain voltage varies from 0V to 1.5V and for the nMOS and pMOS transistors biased with $|V_{GT}|$= 200mV.

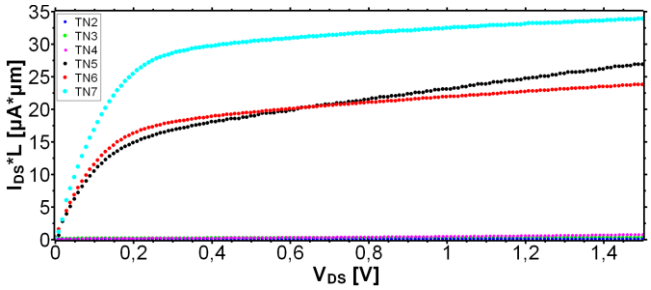

Figure 7 - Shows the results obtained on transistors TN2 to TN7 with constant width of channel W = 3.00µm with varying values of V_{GS} for each transistor. These curves represent the group b).

This analyze demonstrate the difference between the doping concentration. Theoretically, all the parameters of the drain current in triode region (1) are equal, because they are manufactured in the same technology, varying only the channel length between them, the curves should be superimposed. In figure 7, in shorter channel lengths, there is a higher concentration of impurities and thus the drain current is greater compared to a transistor with a longer channel length. By increasing the channel length, the concentration of dopants is decreased and as consequently, the drain current decreases.

Figure 8 gathers a nMOS transistors from TN8 to TN11 with constant channel length L = 1.00µm with V_{GS} values varying according to each transistor. These curves represent the group c).

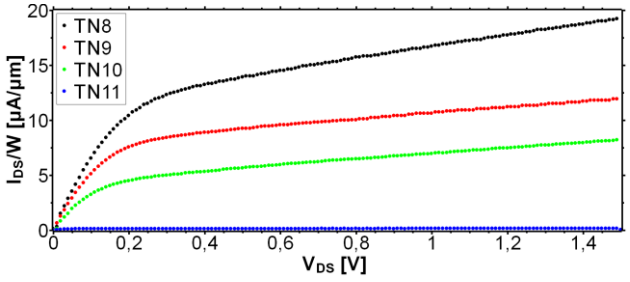

Figure 8 - Shows the results obtained on transistors TN8 to TN11 with constant length of channel L = 1.00µm with varying values of V_{GS} for each transistor. These curves represent the group c).

Through the results in figure 8, it was expected that the curves would be superposed, however due to the concentration of dopants and the fact that the greater the width channel, the greater the amount of impurities in the transistor and as a consequence the drain current is increased.

When the transistor is operating in the saturation region, the drain current follows the equation (2) and because the channel length modulation is very small, the channel length modulation is often considered to be one. During the analysis of the curves, mostly in the pMOS transistors, the curve recedes along the variation of V_{DS}. This retreat is due to the influence of this term.

The results presented demonstrate the influence of carrier mobility and the concentration of impurities in the drain current according to the electrical characteristic of each transistor.

An important part of the work was to identify the difference between nMOS and pMOS drain current.

The drain current from a nMOS transistor has higher values than the drain current from a pMOS. This fact occurs because the nMOS has a higher mobility if compared with the pMOS and the higher the mobility the higher the drain current is.

The figure 9 represents the drain current from a pMOS and nMOS. Besides the mobility and the concentration of impurities, it is possible to say that in the nature, the nMOS has a higher drain current than the pMOS drain current.

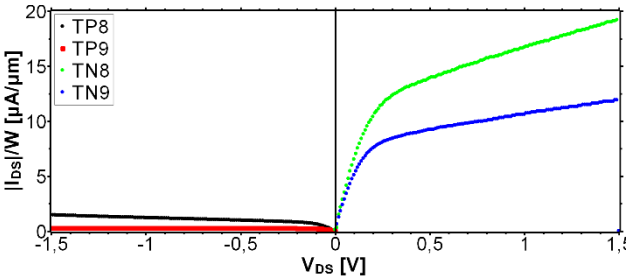

Figure 9 - Shows the results obtained on transistors TN8 and TN9 and TP8 and TP9 with constant length of channel L = 1.00µm with varying values of V_{GS} for each transistor. These curves represent the group c).

III. CONCLUSION

In this work, the electrical characterization of nMOS and pMOS transistors from a CMOS technology with a minimum channel length of 180 nm has been presented. properties were extracted from the obtained curves demonstrated the occurrence of a reduction in the drain current with the reduction of the length and width of the channel, which is associated with an increase in the doping concentration while reducing these dimensions, due to the formation of the pocket region. It was also proof the behavior of the drain current in function of the drain voltage and gate voltage constant and as a result of it, was seen that nMOS devices have a higher drain current than pMOS devices and those were proving by the doping concentration.

This experiment also has shown that even thought the threshold voltage was calculated with the method of second derivate, those voltage do not follow what was expected, i.e., TN2 to TN7 (Group b, Same W but different L). The extracted threshold voltages read: 0.52V, 0.51V, 0.52V, 0.52V, 0.51V, 0.55V) would have higher threhold voltage leading to higher current with the lower channel lenght. This result indicades that during the measuares something went wrong, it could be the lack of contact or during the second derivate analysis.

IV. REFERENCES

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